

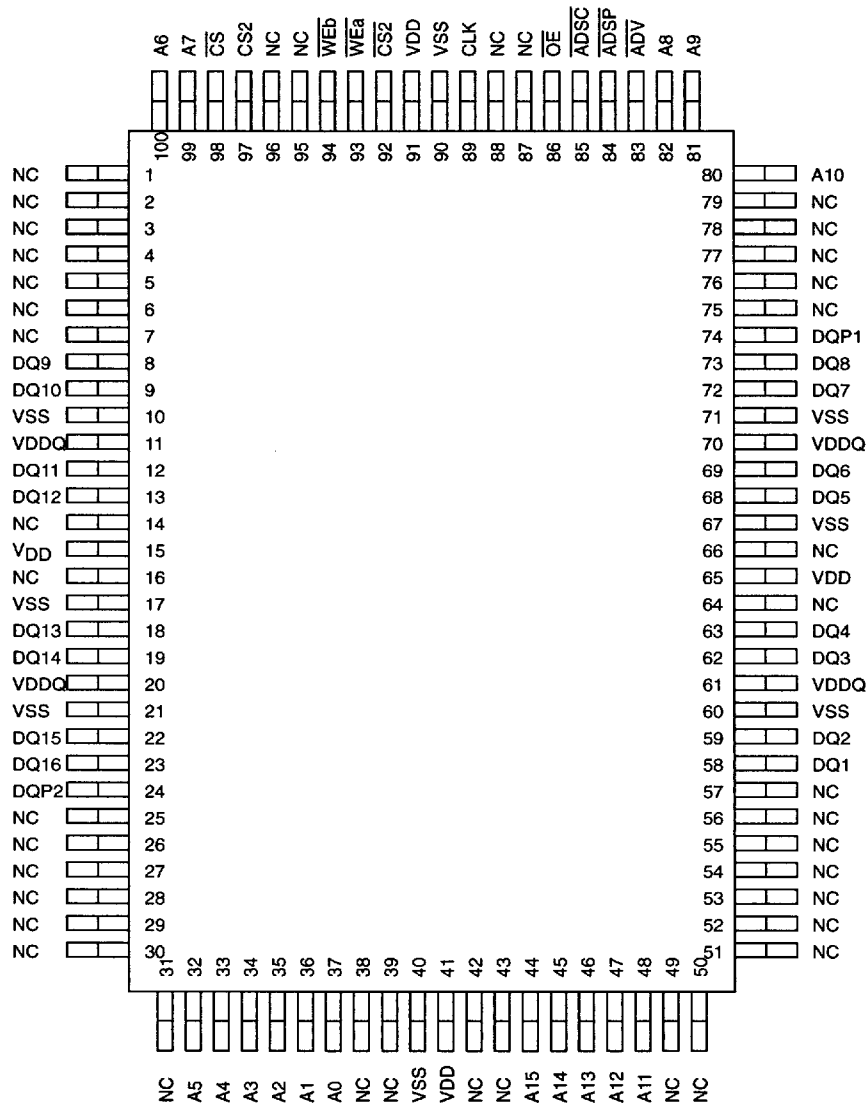
## Features

- 64K x 18 Organization
- 0.5 $\mu$  CMOS Technology
- Synchronous Burst Mode of Operation Compatible with i486™ and Pentium™ Processors
- Supports Pentium™ Processor Address Pipelining
- Common I/O and Registered Outputs
- Single +3.3V  $\pm$  5% Power Supply and Ground
- LVTTTL I/O Compatible
- Fast  $\overline{OE}$  times: 4, 5ns
- Registered Addresses, Data Ins, Control signals, and Outputs
- Asynchronous Output Enable
- Self-Timed Write Operation and Byte Write Capability
- Low Power Dissipation
  - 1.3 W Active at 100MHz
  - 90 mW Standby
- 100 Pin Thin Quad Flat Pack Package
- 5V Tolerant I/O

## Description

IBM Microelectronics 1M SRAM is a Synchronous Burstable Pipelined, high performance CMOS Static RAM that is versatile, wide I/O, and achieves 4 nsec access. A single clock is used to initiate the read/write operation and all internal operations are self-timed. At the rising edge of the Clock, all Addresses, Data Ins and Control Signals are registered internally. Burst mode operation, compatible with the i486™ and Pentium™ Processor's sequence, is accomplished by integrating input registers, internal 2-bit burst counter and high speed SRAM in a single chip. Burst reads are initiated with either ADSP or ADSC being LOW with a valid address during the rising edge of clock. Data from this address plus the three subsequent addresses will be output. The chip is operated with a single +3.3 V power supply and is compatible with LVTTTL I/O interfaces.

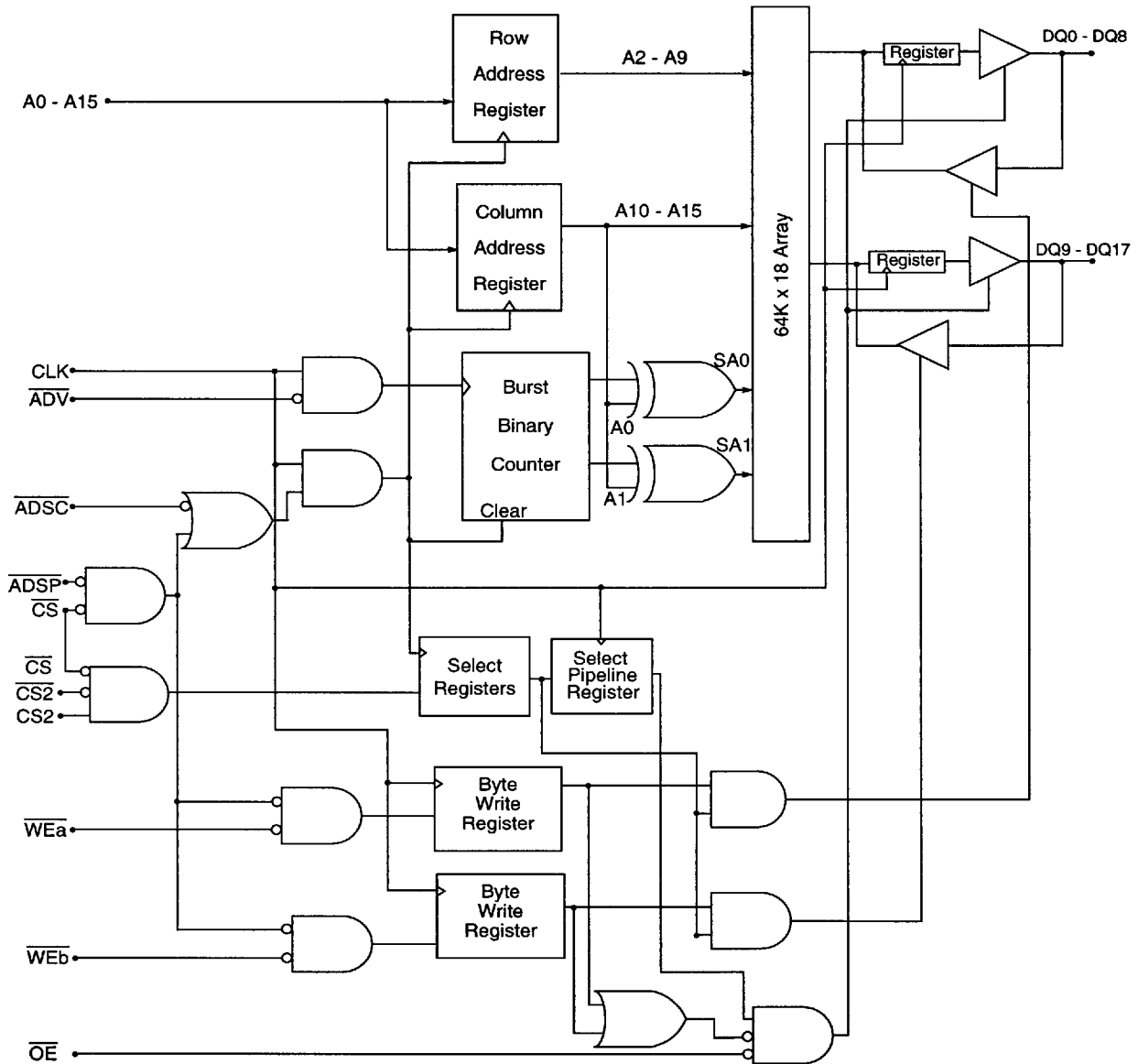
### X18 TQFP Pin Array Layout



### Pin Description

A0-A15	Address input	$\overline{ADSP}$	Address Status Processor
DQa - DQb	Data Input/Output (1-8 , 9-16)	$\overline{ADSC}$	Address status controller
CLK	Clock	$\overline{ADV}$	Burst Advance Control
$\overline{WEa}$	Write Enable, Byte a (1 to 8 & DQP1)	$\overline{CS}$	$\overline{ADSP}$ - Gated Chip Select
$\overline{WEb}$	Write Enable, Byte b (9 to 16 & DQP2)	VDD	Power Supply (+3.3V)
$\overline{OE}$	Output Enable	VSS	Ground
$\overline{CS2}, CS2$	Chip Selects	VDDQ	Output Power Supply (+3.3V)
DQP1,DQP2	Parity bits for byte a, and byte b.	NC	No Connect

### Block Diagram



### Ordering Information

Part Number	Organization	Speed	Leads	Notes
IBM041813PQK-4	64K x 18	4 ns Access / 10 ns Cycle	100 pin TQFP	
IBM041813PQK-5	64K x 18	5 ns Access / 10 ns Cycle	100 pin TQFP	

### Burst SRAM Clock Truth Table

CLK	$\overline{CS2}$	CS2	$\overline{CS}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WE}$	$\overline{OE}$	DQ	Operation
L→H	H	X	L	L	X	X	X	X	HIZ	Deselected Cycle
L→H	X	L	L	L	X	X	X	X	HIZ	Deselected Cycle
L→H	H	X	X	X	L	X	X	X	HIZ	Deselected Cycle
L→H	X	L	X	X	L	X	X	X	HIZ	Deselected Cycle
L→H	L	H	L	L	X	X	X	L	Q	Read from External Address, Begin Burst
L→H	L	H	L	L	X	X	X	H	HIZ	Read from External Address, Begin Burst
L→H	L	H	L	H	L	X	H	L	Q	Read from External Address, Begin Burst
L→H	L	H	L	H	L	X	L	X	D	Write to External Address, Begin Burst
L→H	X	X	X	H	H	L	H	L	Q	Read from next Add., Continue Burst
L→H	X	X	X	H	H	L	L	X	D	Write to next Add., Continue Burst
L→H	X	X	X	H	H	H	H	L	Q	Read from Current Add., Suspend Burst
L→H	X	X	X	H	H	H	L	X	D	Write to Current Add., Suspend Burst
L→H	X	X	H	X	L	X	X	X	HIZ	Deselect Cycle
L→H	X	X	H	X	H	L	H	L	Q	Read from next Add., Continue Burst
L→H	X	X	H	X	H	L	L	X	D	Write to next Add., Continue Burst
L→H	X	X	H	X	H	H	H	L	Q	Read from current Add., Suspend Burst
L→H	X	X	H	X	H	H	L	X	D	Write to current Add., Suspend Burst

1. For a write operation preceded by a read cycle,  $\overline{OE}$  must be HIGH early enough to allow Input Data Setup, and must be kept HIGH through Input Data Hold Time.
2.  $\overline{WE}$  refers to  $\overline{WEa}$ ,  $\overline{WEb}$ .
3.  $\overline{ADSP}$  is gated by  $\overline{CS}$ , and  $\overline{CS}$  is used to block  $\overline{ADSP}$  when  $\overline{CS} = V_{IH}$ , as required in applications using Processor Address Pipelining.
4. All Addresses, Data In and Control signals are registered on the rising edge of CLK.
5. Write cycles will put the bus into HIZ on the first rising clock edge according to the Tchz timing. Deselect cycles will put the bus into HIZ on the second rising edge of clock according to the Tchz timing. If a deselect cycle occurs and  $\overline{WE}$  is enabled within the same cycle, the part behaves as though it was in a deselect cycle.

### Burst Sequence Truth Table

External Address	A15-A2	(A1,A0)				Notes
		(0,0)	(0,1)	(1,0)	(1,1)	
1st Access	A15-A2	(0,0)	(0,1)	(1,0)	(1,1)	
2nd Access	A15-A2	(0,1)	(0,0)	(1,1)	(1,0)	
3rd Access	A15-A2	(1,0)	(1,1)	(0,0)	(0,1)	
4th Access	A15-A2	(1,1)	(1,0)	(0,1)	(0,0)	

### Write Enable Truth Table

$\overline{WEa}$	$\overline{WEb}$	Byte Written	Notes
H	H	Read All Bytes	
L	L	Write All Bytes	
L	H	Write Byte A (D <sub>IN</sub> 0 - 8)	
H	L	Write Byte B (D <sub>IN</sub> 9 - 17)	

### Absolute Maximum Ratings

Parameter	Symbol	Rating	Units	Notes
Power Supply Voltage	V <sub>DD</sub>	-0.5 to 4.6	V	1
Input Voltage	V <sub>IN</sub>	-0.5 to 6.0	V	1
Output Voltage	V <sub>OUT</sub>	-0.5 to V <sub>DD</sub> +0.5	V	1
Operating Temperature	T <sub>OPR</sub>	0 to +70	°C	1
Storage Temperature	T <sub>STG</sub>	-55 to +125	°C	1
Power Dissipation	P <sub>D</sub>	2.0	W	1
Short Circuit Output Current	I <sub>OUT</sub>	50	mA	1

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

### Recommended DC Operating Conditions (T<sub>A</sub>=0 to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Supply Voltage	V <sub>DD</sub>	3.135	3.3	3.465	V	1,4
Input High Voltage	V <sub>IH</sub>	2.2	—	5.5	V	1,2,4
Input Low Voltage	V <sub>IL</sub>	-0.3	—	0.8	V	1,3,4
Output Current	I <sub>OUT</sub>	—	5	8	mA	4

- All voltages referenced to V<sub>SS</sub>. All V<sub>DD(Q)</sub> and V<sub>SS(Q)</sub> must be connected.
- V<sub>IH</sub>(Max)DC = 5.5 V, V<sub>IH</sub>(Max)AC = 6.0 V (pulse width ≤ 4.0ns)
- V<sub>IL</sub>(Min)DC = - 0.3 V, V<sub>IL</sub>(Min)AC = -1.5 V (pulse width ≤ 4.0ns)
- Input voltage levels are tested to the following DC conditions: 1 microsecond cycle and 200 ns set-up and hold times

### Capacitance (T<sub>A</sub>=0 to +70°C, V<sub>DD</sub>=3.3V ± 5%, f=1MHz)

Parameter	Symbol	Test Condition	Max	Units	Notes
Input Capacitance	C <sub>IN</sub>	V <sub>IN</sub> = 0V	5	pF	
Data I/O Capacitance (DQ0-DQ17)	C <sub>OUT</sub>	V <sub>OUT</sub> = 0V	5	pF	

### DC Electrical Characteristics (T<sub>A</sub>= 0 to +70°C, V<sub>DD</sub>=3.3V ± 5%)

Parameter	Symbol	Min.	Max.	Units	Notes
Operating Current Average Power Supply Operating Current (I <sub>OUT</sub> = 0, OE = V <sub>IH</sub> .)	I <sub>DD10</sub>	—	375	mA	2,3
Standby Current Power Supply Standby Current (CS2 = V <sub>IH</sub> or CS2 = V <sub>IL</sub> or CS = V <sub>IL</sub> All other inputs = V <sub>IH</sub> or V <sub>IL</sub> , I <sub>OUT</sub> = 0 Clock @ 100 MHz)	I <sub>SB</sub>	—	25	mA	1,3
Input Leakage Current Input Leakage Current, any input (V <sub>IN</sub> = 0 & V <sub>DD</sub> )	I <sub>LI</sub>	—	+1	μA	4
Output Leakage Current (V <sub>OUT</sub> = 0 & V <sub>DD</sub> , OE = V <sub>IH</sub> )	I <sub>LO</sub>	—	+1	μA	
Output High Level Output "H" Level Voltage (I <sub>OH</sub> =-8mA @ 2.4V)	V <sub>OH</sub>	2.4	—	V	
Output Low Level Output "L" Level Voltage (I <sub>OL</sub> =+8mA @ 0.4V)	V <sub>OL</sub>	—	0.4	V	

- I<sub>SB</sub> = Stand-by Current
- I<sub>DD</sub> = Selected Current
- I<sub>OUT</sub> = Chip Output Current
- The input leakage current for 5.5V input is 200 μA for Clk, Chip Selects, and Output Enable. Other inputs have 100 μA of leakage current at 5.5V

**AC Test Conditions** ( $T_A=0$  to  $+70^\circ\text{C}$ ,  $V_{DD}=3.3\text{V} \pm 5\%$ )

Parameter	Symbol	Conditions	Units	Notes
Input Pulse High Level	$V_{IH}$	3.0	V	
Input Pulse Low Level	$V_{IL}$	0.0	V	
Input Rise Time	$T_R$	2.0	ns	
Input Fall Time	$T_F$	2.0	ns	
Input and Output Timing Reference Level		1.5	V	
Output Load Conditions				1

1. See AC Test Loading figure on page 9.

**AC Characteristics** ( $T_A=0$  to  $+70^\circ\text{C}$ ,  $V_{DD}=3.3\text{V} \pm 5\%$ , Units in nsec)

Parameter	Symbol	-4		-5		Notes
		Min.	Max.	Min.	Max.	
Cycle Time	$t_{\text{CYCLE}}$	10.0	—	10.0	—	
Clock Pulse High	$t_{\text{CH}}$	3.0	—	3.0	—	
Clock Pulse Low	$t_{\text{CL}}$	3.0	—	3.0	—	
Clock to Output Valid	$t_{\text{CQ}}$	—	4.0	—	5.0	1
Address Status Controller Setup Time	$t_{\text{ADSCS}}$	2.5	—	2.5	—	
Address Status Controller Hold Time	$t_{\text{ADSCH}}$	0.5	—	0.5	—	
Address Status Processor Setup Time	$t_{\text{ADSPS}}$	2.5	—	2.5	—	
Address Status Processor Hold Time	$t_{\text{ADSPH}}$	0.5	—	0.5	—	
Advance Setup Time	$t_{\text{ADVS}}$	2.5	—	2.5	—	
Advance Hold Time	$t_{\text{ADVH}}$	0.5	—	0.5	—	
Address Setup Time	$t_{\text{AS}}$	2.5	—	2.5	—	
Address Hold Time	$t_{\text{AH}}$	0.5	—	0.5	—	
Chip Selects Setup Time	$t_{\text{CSS}}$	2.5	—	2.5	—	
Chip Selects Hold Time	$t_{\text{CSH}}$	0.5	—	0.5	—	
Write Enables Setup Time	$t_{\text{WES}}$	2.5	—	2.5	—	
Write Enables Hold Time	$t_{\text{WEH}}$	0.5	—	0.5	—	
Data In Setup Time	$t_{\text{DS}}$	2.5	—	2.5	—	
Data In Hold Time	$t_{\text{DH}}$	0.5	—	0.5	—	
Data Out Hold Time	$t_{\text{CQX}}$	0.75	—	0.75	—	1
Clock High to Output High Z	$t_{\text{CHZ}}$	—	5.0	—	5.5	1,2,3
Clock High to Output Active	$t_{\text{CLZ}}$	0.5	—	0.5	—	1,2,3
Output Enable to High Z	$t_{\text{OHZ}}$	2.0	6.0	2.0	6.5	1,2
Output Enable to Low Z	$t_{\text{OLZ}}$	0.25	—	0.25	—	1,2
Output Enable to Output Valid	$t_{\text{OQ}}$	—	4.0	—	5.0	1

1. See AC Test Loading figure 1 on page 11.
2.  $T_{\text{OHZ}}$ ,  $T_{\text{OLZ}}$ ,  $T_{\text{CHZ}}$  and  $T_{\text{CLZ}}$  transitions are measured  $\pm 200$  mV from steady state voltage. See AC Test Loading figure 2 on page 11.
3. In depth expansion applications where one SRAM is selected and the other is not, bus contention will not occur because  $T_{\text{clz}}$  is measured from the second rising clock edge while  $T_{\text{chz}}$  is measured from the first rising clock edge.



### AC Test Loading

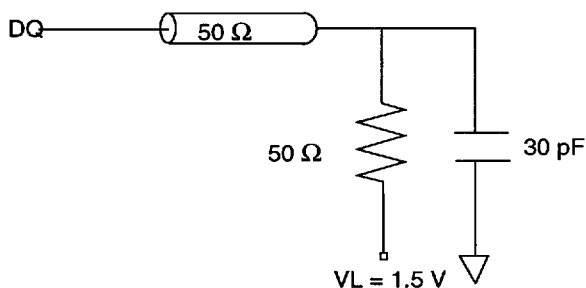


Fig. 1 Test Equivalent Load

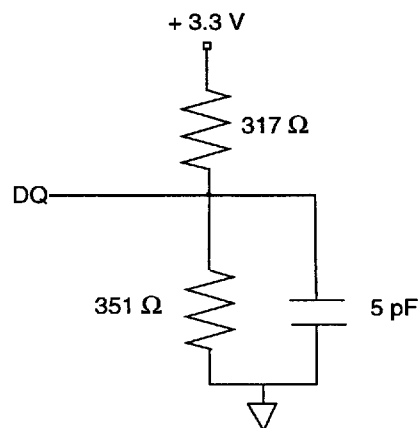
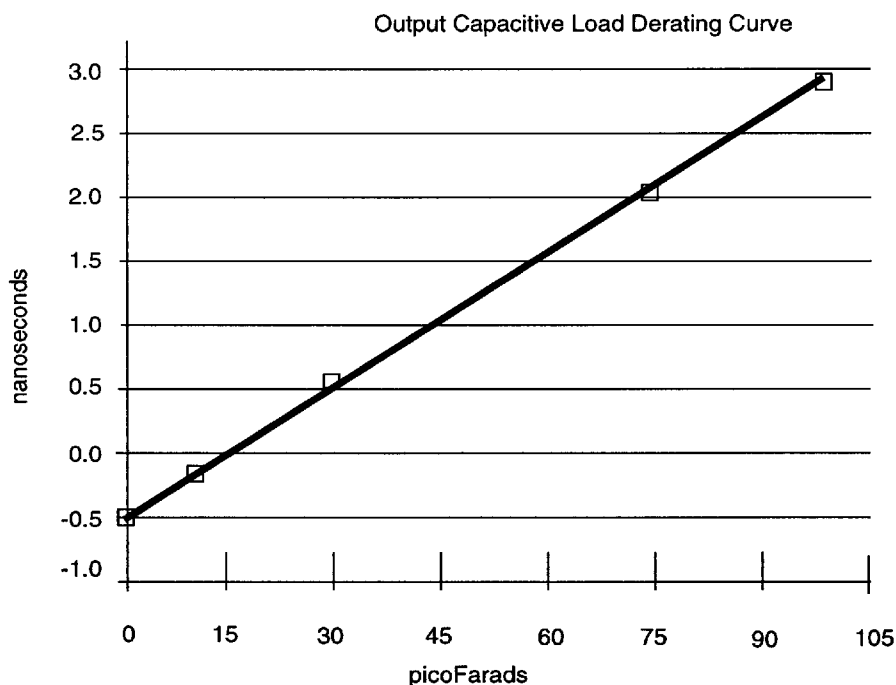
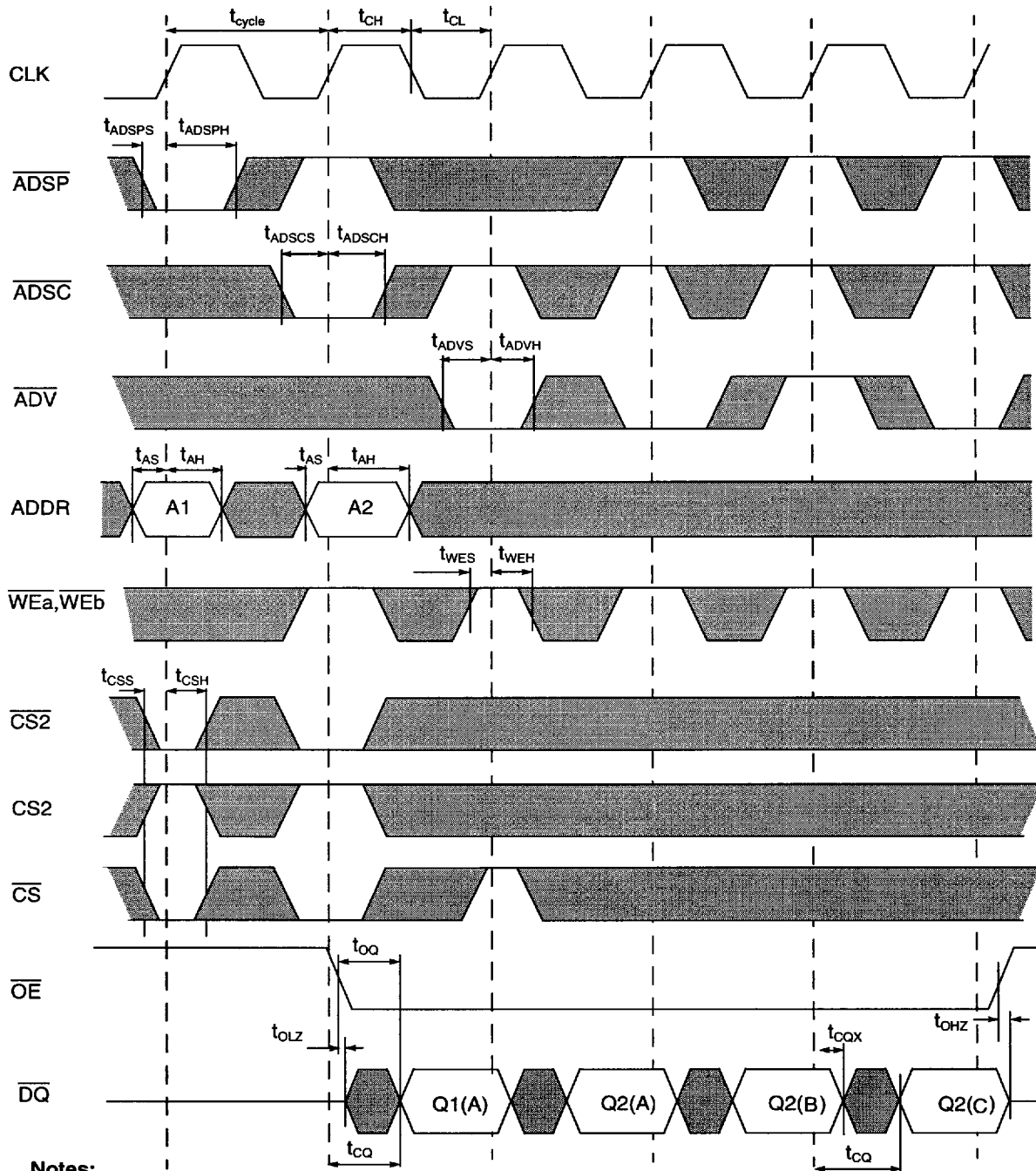


Fig. 2 Test Equivalent Load



The derating curve above is for a purely capacitive load on the output driver. For example, a part specified at 4 ns access time will behave as though it has a 4.5 ns access time if a 30 pF load with no DC component was attached to the output driver. The access times guaranteed in the datasheets are based on a 50 ohm terminated test load. For unterminated loads the derating curve should be used. This curve is based on nominal process conditions with worst case parameters  $V_{cc} = 3.14 \text{ V}$ ,  $T_a = 70^\circ \text{ C}$ .

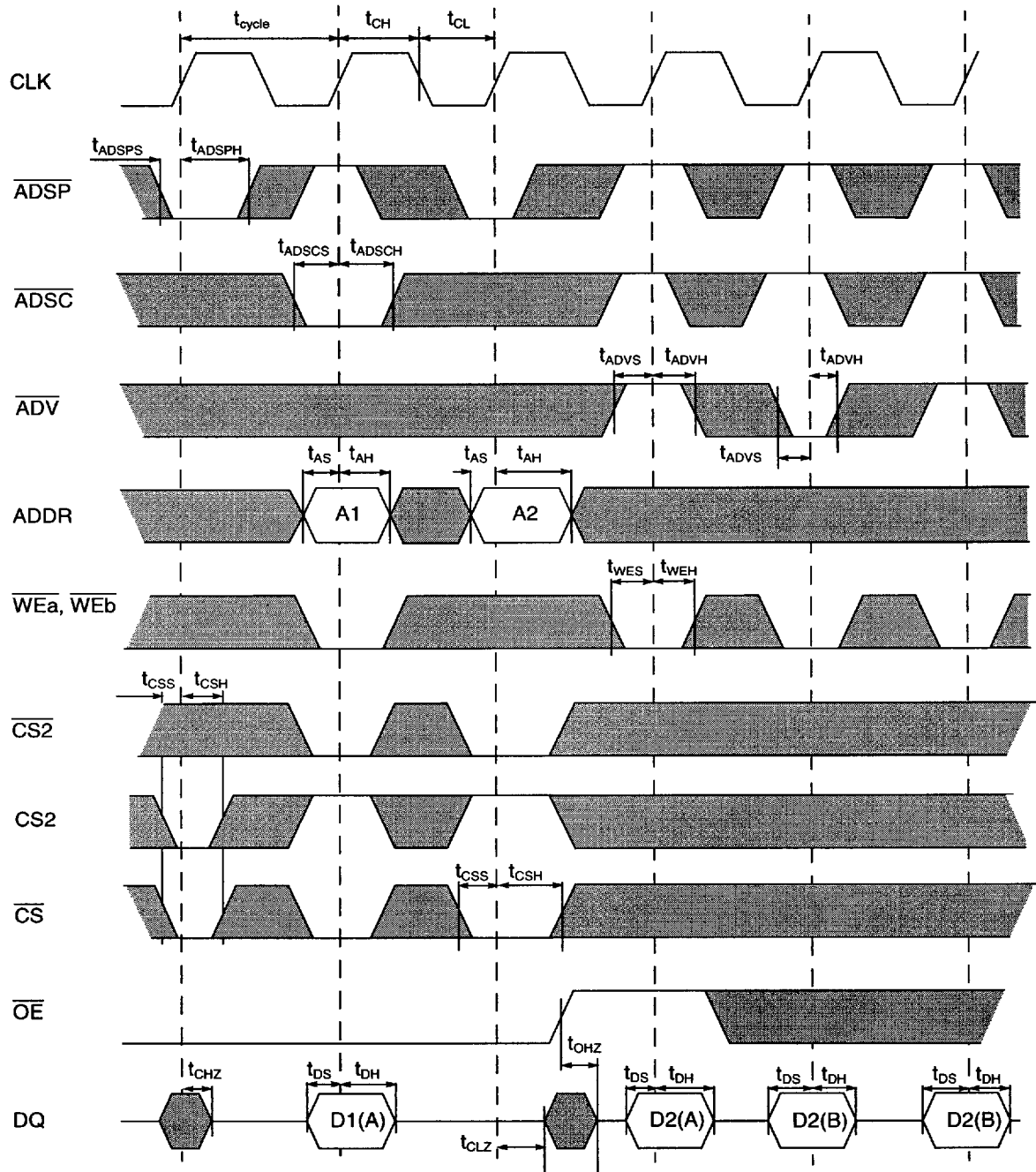
### Timing Diagram (Burst Read)



**Notes:**

1. Q1(A) and Q2(A) refer to data read from address A1 and A2.
2. Q2(B), Q2(C) and Q2(D) refer to data read from subsequent internal burst counter addresses.

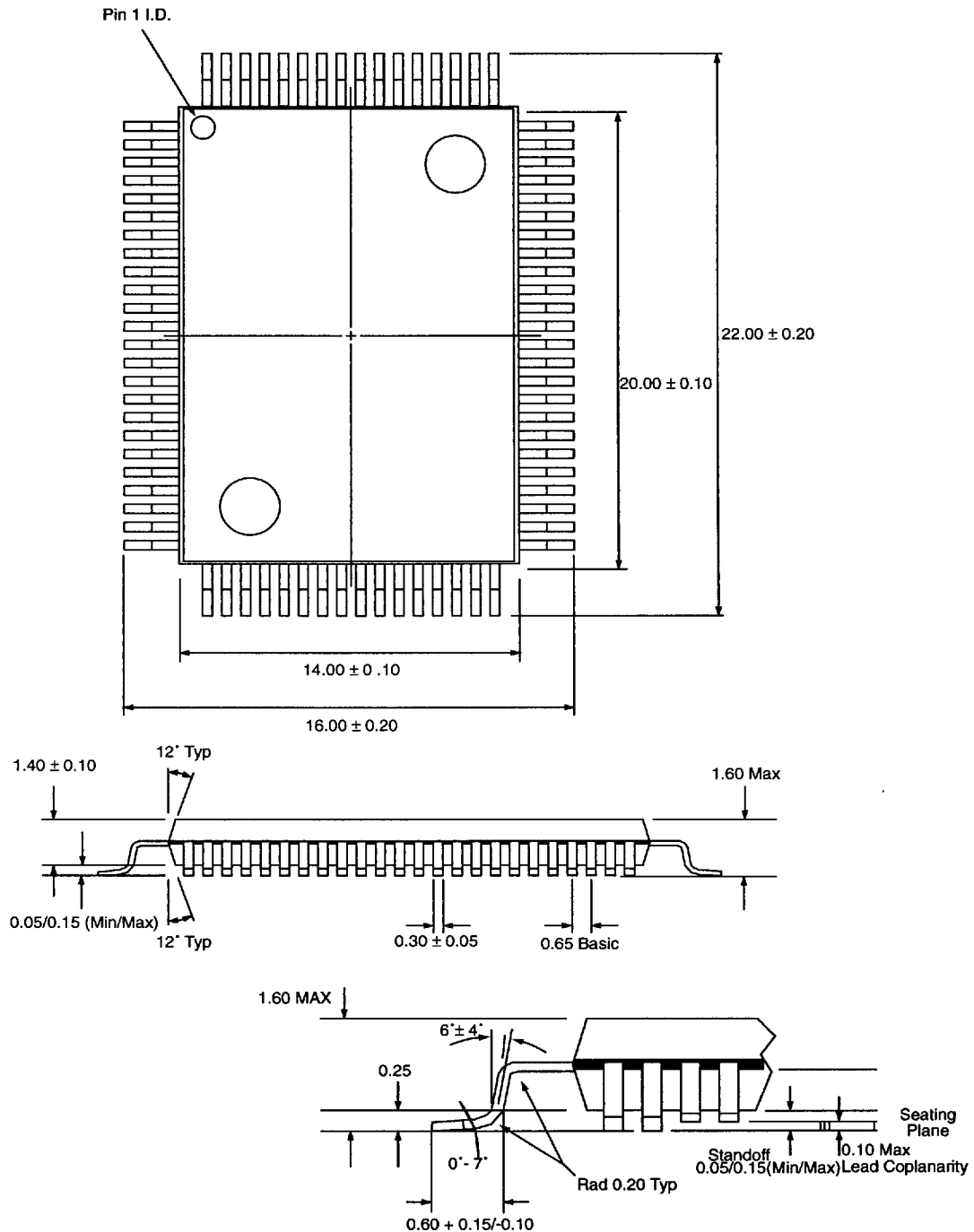
**Timing Diagram (Burst Write)**



**Notes:**

1. D1(A) and D2(A) refer to data written to address A1 and A2.
2. D2(B) refers to data written to a subsequent internal burst counter address.
3. WEa, WEb are don't cares when ADSP is sampled LOW.

### 100 Pin TQFP Package Diagram



**Connect Compatibility for 64K x18 and Future 64K x 16 & 64K x 18**

TQFP PIN #	Current Connections (x18)	Future Connections (x16 & x18)	Function
4,27,54,77	NC	Vddq	Output Power Supply
5,26,55,76	NC	Vss	Ground
14	NC	Low or High, NC for most vendors but Low or High to comply to the JEDEC standard.	$\overline{FT}$ , FLow thru or Pipeline function, tie Low for flow thru, High for Pipeline
24	DQP2	NC or DQ in x18	Parity bit for second byte
31	NC	Low or High	$\overline{LB}$ Linear Burst Order, This pin must be tied low for linear(PowerPC), High for Interleave (Pentium)
64	NC	Low or High. Low allows normal operation.	$\overline{ZZ}$ , Asynchronous Sleep Mode, Tie to ground for normal function, Vddq for sleep mode (Low power state)
74	DQP1	NC or DQ in x18	Parity bit for first byte
87	NC	Low or $\overline{BWE}$ , Tie low if function not used	Byte Write Enable, Allows individual bytes to be written.
88	NC	Low or $\overline{GW}$ , Tie High if function not used	Global Write Enable, Allows write of all bytes to occur with single pin.

The IBM041813PQK has the pins connected in the manner indicated in the Current Connections (x18) and is also JEDEC complaint. Future Connections refers to the evolution on the JEDEC standard for subsequent part numbers.

## Revision Log

Rev	Contents of Modification
4/95	Initial Release of the 64K x 18 (10/12) TQFP BURST PIPELINE MODE Application Spec.
7/95	Added Note 5 on Burst SRAM Clock Truth Table & Note 3 on AC Characteristics for clarification purposes. Updated AC Characteristics as well.
3/96	Upgraded the cycle time for the -12 part from 12ns cycle to 10ns cycle. Also changed the part number to read -access instead of -cycle because now both IBM041813PQK parts have 10ns cycle time.